



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani et al. Art Unit : 2815
Serial No. : 09/379,702 Examiner : Eugene Lee
Filed : August 24, 1999
Title : METHOD OF FABRICATING SEMICONDUCTOR DEVICES

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Pursuant to 37 CFR 1.193(b)(1), Appellant responds to the new points raised in the Examiner's Answer dated December 28, 2004 as follows.

Appellant disagrees with the arguments in the Answer that the application does not discuss the importance of having a side of the first insulating film aligned with the side of the crystalline semiconductor island. As set forth in the application, the process for forming a semiconductor device according to Figs. 1A-1E has numerous advantages that result in an improved device. For example, the first gate insulating film serves to prevent the crystalline silicon film from being contaminated after deposition of an amorphous silicon film (see the application at the last line of page 25 through page 26, line 7), serves as a capping layer for suppressing generation of ridges due to laser light, and serves as an antireflective film for laser light by appropriately controlling its thickness (page 9, third paragraph through page 11, line 6 and Fig. 5). To serve these functions, the first insulating film is in place during formation of the semiconductor island and, as a result, the first insulating film has a side aligned with the side of the semiconductor island.

The second gate insulating film then is formed so that a combination of the first and second gate insulating films has a thickness suitable to function as a gate insulating film in a thin film transistor. Since the second gate insulating film is formed on the first gate insulating film after formation of the semiconductor island, the second gate insulating film extends beyond an edge of the first gate insulating film. Thus, the structure recited in the independent claims is one that results from using the advantageous process described with respect to Figs. 1A-1E.

The Answer indicates that the appellant's discussion of why a person of ordinary skill in the art would have been more likely to take the first approach noted in the appeal brief than the

fourth approach is not persuasive because the methods used are not an issue with respect to the claimed apparatus. However, as illustrated above, the method used will significantly impact the resulting apparatus. In particular, as discussed in the appeal brief, only the fourth approach could be used to produce an apparatus that includes insulating layers arranged in the manner recited in the claims. Accordingly, appellant respectfully submits that the discussion provided in the appeal brief as to which approach a person of ordinary skill in the art would have been likely to use in view of Yamazaki and Matsumoto needs to be considered. As set forth in that discussion, Matsumoto's description of the benefits of having a thicker gate insulating film would not have led one of ordinary skill in the art to adopt the fourth approach and, accordingly, would not have led to the production of a device that falls within the claimed subject matter.

The Answer also indicates that appellant's discussion of the likelihood of adopting one approach over the other is based on speculation, and "does not preclude the fact that Matsumoto has provided a clear motivation (increase the on-voltage and suppress an increase in current consumption) to include an interlayer insulating film over Yamazaki's gate insulating film 3." Appellant strongly disagrees. Matsumoto has provided no such "clear motivation." Rather, Matsumoto, at best, provides motivation for increasing the thickness of the gate insulating film. As set forth in the appeal brief, there are several ways to accomplish this that are far more straightforward than the one suggested in the rejection, such that one of ordinary skill in the art would have been motivated to select a more straightforward approach and would not have been motivated to select the approach that would result in a device such as is recited in the claims.

For these reasons, and the reasons stated in the Appeal Brief, appellant submits that the final rejection should be reversed.

Please apply any charges or credits to Deposit Account No. 06-1050.

Applicant : Hisashi Ohtani et al.
Serial No. : 09/379,702
Filed : August 24, 1999
Page : 3 of 3

Attorney's Docket No.: 07977-093002 / US3164D1

Respectfully submitted,

Date: 2/28/05


John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331



Attorney's Docket No. 07977-093002		Mailing Date February 28, 2005
Application No. 09/379,702	Filing Date August 24, 1999	Attorney/Secretary Init JFH/cmt
Title of the Invention METHOD OF FABRICATING SEMICONDUCTOR DEVICES		
Applicant Hisashi Ohtani et al.		
Client Reference No. US3164D1		
Enclosures		
<p>➤ Reply Brief (3 pages)</p> <p>FR</p>		
<p>For PTO Use Only Do Not Mark in This Area</p>		